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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,074	11/19/2003	Peter Dean Swartz	GENSP052	1073

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EXAMINER	
RICHER, AARON M	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,074	SWARTZ ET AL.	
	Examiner	Art Unit	
	AARON M. RICHER	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,7-10,12-14,18-23,25 and 29-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-10,12-14,18-23,25 and 29-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-3, 7-10, 12-14, 18-23, 25, and 29-34 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-3, 7-10, 12-14, 18-23, 25, and 29-34 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Claim 1 recites a configurable frame rate conversion unit configured to synchronize each converted data stream to an output frame rate, wherein the output frame rate is selectively locked to any of the input video data stream clock rates or a ration of the input video stream clock rates, and not a display clock rate. Claims 12 and 23 recite similar limitations. However, figure 2 of applicant's specification clearly shows that there is a "progressive display clock" and p. 17, section 0032 of applicant's specification shows that this clock runs at the display rate of the display and is used to convert streams to a progressive timing at that rate. Applicant does not appear to have

support in the specification for locking to an input clock rate or ratio and **not** a display clock rate.

5. Applicant states that original claim 4 gives support for the new limitations of claim 1, but original claim 4 did not contain a limitation about converting to a rate that is "not a display clock rate". Applicant also points to section 0029 of the specification as having support for this limitation, but this section simply discusses the bi-directional link and not any frame rate conversion.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-3, 8-10, 12-14, 19-23, and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perlman (U.S. Publication 2002/0135696) in view of Shigeta

(U.S. Publication 2002/0089518) and further in view of Elliott (U.S. Publication 2002/0054031).

9. As to claims 1, 12, and 23, as best understood, Perlman discloses a video processor for providing a single synchronized video stream having a single display video format to a first display device having a first set of display attributes from a number of input video streams of different video formats, comprising:

a number of ports each of which is configured to receive one of the input video streams at a corresponding input video stream clock rate (fig. 2; p. 2, section 0020; multiple communication modules for receiving data are disclosed; these read on ports);

a number of configurable image converter units each coupled to an associated one of the ports for converting the corresponding input video stream to a corresponding converted video stream having the single display video format that is based upon the set of display attributes (fig. 3a; fig. 3b; the units are configurable based on input format and attributes of a display);

and a system controller unit in communication with each of the configurable image converter units arranged to configure the image converter units in real time, wherein each of the configured image converter units convert the corresponding input video signal to the corresponding converted video stream having the single display video format (fig. 3a-3b; conversion is reconfigured if an interlaced display is replaced with a progressive one or vice versa).

Perlman does not disclose a frame rate conversion unit configured to synchronize each converted data stream to a selected output frame rate. Shigeta,

however, discloses a system which uses DDC or EDID to determine a display's attributes and then synchronizes streams to a given frame rate (p. 6, sections 0090-0094). The motivation for this is to be able to display computer content on TV monitors and TV content on computer monitors (p. 1, section 0005-0006). It would have been obvious to one skilled in the art to modify Perlman to synchronize converted data streams to a selected output frame rate in order to efficiently convert content for a TV or PC monitor as taught by Shigeta.

Neither Perlman nor Shigeta disclose a frame rate conversion unit that an output frame rate is locked to an input video clock rate rather than a display clock rate. Elliott, however, discloses a display system that locks an output frame rate to an input frame rate, which an input video is converted/synchronized to, regardless of a display rate (p. 2, section 0013). Elliott enables this by changing a display frame rate to suit an input frame rate instead of the usual method of changing an input frame rate to a display frame rate. The motivation for this is to avoid the artifacts that come with synchronizing an input rate to a display rate (p. 1, section 0010). It would have been obvious to one skilled in the art to modify Perlman and Shigeta to convert to one of the input frame rates rather than a display frame rate in order to avoid artifacts as taught by Elliott.

10. As to claims 2, 13, and 34, Perlman discloses a configurable real time video processor wherein when a second display unit having a second set of display attributes replaces the first display unit, then the system controller uses the second set of display attributes received from the second display unit to reconfigure the configurable image converter units and the configurable frame rate conversion unit accordingly (fig. 3a-3b;

conversion is reconfigured if an interlaced display is replaced with a progressive one or vice versa).

11. As to claims 3, 14, and 25, Perlman discloses a processor comprising:

an image compositor unit arranged to combine the converted data streams to form a composited data stream (fig. 3a, element 312);

an image enhancer unit arranged to enhance the composited data stream to form an enhanced data stream (p. 2-3; section 0026; an anti-aliased composited stream reads on an "enhanced" data stream);

a display unit interface arranged process the enhanced data stream to form the display data (fig. 3a, element 314);

and a memory unit bi-directionally coupled to each of the image converter units and the image compositor arranged to store selected portions of selected ones of the data streams from the image converter units and to provide the selected portions to the image compositor as needed (fig. 2, element 216; p. 2-3; section 0026; buffers hold the foreground and background pixels to be combined).

12. As to claims 8, 19, and 30, Perlman discloses

a video receiver port arranged to receive video data at a video clock rate (fig. 2, element 230);

a bi-directional network interface arranged to receive network data from network applications on a network, and transmit data to the network from the real time video processor at a network data clock rate (fig. 2, element 220; a clock rate for data transfer is inherent);

a user interface port arranged to receive user input commands at a user interface clock rate (p. 2, sections 0022-0025; a user interface is disclosed; also note "interactive" content in fig. 2).

13. As to claims 9, 20, and 31, none of Perlman, Shigeta, and Elliott discloses a processor as an integrated circuit. Official notice has been taken of the fact that graphics processors on integrated circuits are well-known in the art (see MPEP 2144.03). It would have been obvious to one skilled in the art to modify Perlman, Shigeta, and Elliott to use an integrated circuit in order to make the graphics processor smaller and reduce production costs.

14. As to claims 10, 21, and 32, Shigeta discloses basing conversion on a set of Extended Display Identification Data (EDID) attributes (p. 6, sections 0090-0093; EDID data is read and then used to convert parameters such as frame rate and resolution). The motivation for combination of Shigeta and Perlman can be found in the rejection to claim 1.

15. As to claims 11, 22, and 33, Perlman discloses

an interlacer unit arranged to interlace a progressive scan image when the display unit is an interlaced type display unit (p. 3, section 0028; the flicker filter formats a progressive image for an interlaced display);

and a progressive scan bypass unit arranged to bypass the interlacer when the display unit is a progressive scan type display unit (fig. 3a, no interlacer is used).

16. Claims 7, 18, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perlman in view of Shigeta and Elliott and further in view of Naegle (U.S. Publication 2004/0012577).

17. As to claims 7, 18, and 29, none of Perlman, Shigeta, and Elliott expressly discloses a processor wherein the display frame rate is a free running frame rate. Naegle, however, does disclose a video processor with a free running frame rate. The motivation for this is to provide a larger set of pixel clock frequencies for various formats (p. 1, paragraph 0014). It would have been obvious to one skilled in the art to modify Perlman, Shigeta, and Elliott to use a free running frame rate in order to support more diverse formats as taught by Naegle.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AARON M. RICHER whose telephone number is (571)272-7790. The examiner can normally be reached on weekdays from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AMR
3/16/08

/Kee M Tung/
Supervisory Patent Examiner, Art Unit 2628